

WE CLAIM:

1. A memory cell, comprising:

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providing a PMOS drive transistor with a gate terminal, a first source/drain terminal, and a second source/drain terminal;

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providing a NMOS pass transistor with a gate terminal, a first source/drain terminal and a second source/drain terminal;

connecting said first source/drain terminal of said NMOS pass transistor to a bitline;

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connecting said second source/drain terminal of said NMOS pass transistor to a first storage node;

connecting said gate terminal of said NMOS pass transistor to a wordline;

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connecting said first source/drain terminal of said PMOS drive transistor to a supply voltage;

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connecting said second source/drain terminal of said PMOS drive transistor to said first storage node;

connecting said gate terminal of said PMOS drive transistor to a second storage node; and

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wherein a current flowing through the source/drain terminals of the NMOS pass transistor is greater than a current flowing through the source/drain terminals of the PMOS drive

transistor for the same voltages applied between the gate and source/drain terminals of the PMOS drive transistor and the gate and source/drain terminals of the NMOS pass transistor.

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2. The memory cell of claim 1 wherein during a read operation a voltage applied to the wordline is less than 90% of the supply voltage.

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